

CLAIMS

1. A method comprising steps of:

forming a layer over a transistor gate and a field oxide region;

doping with a first dopant said layer over said transistor gate without doping said

5 layer over said field oxide region:

doping said layer over said transistor gate and said field oxide regions with a

second dopant so as to form a resistor in said layer over said field oxide region.

2. The method of claim 1 further comprising a step of fabricating a contact

10 region for said resistor.

3. The method of claim 1 wherein said layer comprises polycrystalline silicon.

4. The method of claim 1 wherein said transistor gate is a gate of a PFET.

5. The method of claim 1 wherein said transistor gate is a gate of an NFET.

6. The method of claim 1 wherein said field oxide comprises silicon dioxide.

20 7. The method of claim 1 wherein said first dopant is an N type dopant.

8. The method of claim 7 wherein said N type dopant comprises phosphorous.

*2nd  
C3*  
9. The method of claim 1 wherein said first dopant comprises phosphorous at a dose of approximately  $6.5 \times 10^{15}$  atoms per square centimeter.

5 10. The method of claim 1 wherein said second dopant is a P type dopant.

11. The method of claim 10 wherein said P type dopant comprises boron.

*Part 10*  
12. The method of claim 1 wherein said second dopant comprises boron at a dose of approximately  $1.0 \times 10^{15}$  atoms per square centimeter.

13. The method of claim 2 wherein said contact region comprises a silicide.

*14.* A method comprising steps of:  
depositing a polycrystalline silicon layer on a chip;  
forming a doping barrier above said polycrystalline silicon layer so as to prevent doping of a resistor region of said polycrystalline silicon layer;  
doping said polycrystalline silicon layer with a first dopant;  
removing said doping barrier;  
20 doping said polycrystalline silicon layer with a second dopant.

15. The method of claim 14 wherein said doping barrier comprises photoresist.

16. The method of claim 14 wherein said polycrystalline silicon layer includes a  
gate region.

17. The method of claim 14 wherein said step of doping said polycrystalline  
silicon layer with a first dopant comprises doping said gate region.

18. The method of claim 14 wherein said first dopant is an N type dopant.

19. The method of claim 18 wherein said N type dopant comprises  
phosphorous.

20. The method of claim 14 wherein said first dopant comprises phosphorous at  
a dose of approximately  $6.5 \times 10^{15}$  atoms per square centimeter.

21. The method of claim 14 wherein said second dopant is a P type dopant.

22. The method of claim 21 wherein said P type dopant comprises boron.

23. The method of claim 14 wherein said second dopant comprises boron at a  
dose of approximately  $1.0 \times 10^{15}$  atoms per square centimeter.

24. The method of claim 14 further comprising a step of fabricating a contact

region electrically connected to said resistor region.

25. The method of claim 24 wherein said contact region comprises a silicide.

卷之三